In the Claims

The claims have been amended as follows:

1. (original) A method of providing an array top oxide over an array of trenches containing trench capacitors and overlying vertical transistors comprising:

providing a substrate having a first area and a second area;

providing a sacrificial oxide layer over said first and second areas;

removing said sacrificial oxide layer only from said second area;

providing a gate oxide layer over said second area;

depositing a gate conductor layer over said first and second areas;

removing said gate conductor layer only from said first area;

depositing an array top oxide layer over said first and second areas; and

removing said array top oxide layer from said second area so as to leave remaining portions of said array top oxide layer only in said first area.

2. (original) The method of claim 1 wherein said first area comprises an array area.

3. (original) The method of claim 1 wherein said second area comprises a support area.

4. (Currently amended~~original~~) The method of claim 1 further including, prior to said step of providing ~~growing~~ said sacrificial oxide layer, the steps of:

removing a pad nitride layer in both said first and second areas to expose a pad oxide layer in both said first and second areas;

removing at least a portion of said pad oxide layer from both said first and second areas; and

growing said sacrificial oxide layer over exposed surface areas of said substrate.

5. (original) The method of claim 4 further including, after said step of growing said sacrificial oxide layer, implanting said first and second areas.

6. (Currently amended~~original~~) The method of claim 1 wherein said step of removing said sacrificial oxide layer only from said second area comprises:

removing said sacrificial oxide layer only from said second area wherein a mask is provided over said first area to protect said first area during said sacrificial oxide layer removal processing; and

removing said mask from said first area prior to providing said gate oxide layer over said second area.

7. (Currently amended~~original~~) The method of claim 1 wherein said step of removing said gate conductor layer only from said first area comprises:

removing said gate conductor layer only from said first area wherein a mask is provided over said second area to protect said second area during said gate conductor layer removal processing; and

removing said mask from said second area prior to depositing said array top oxide layer.

8. (Currently amended~~original~~) The method of claim 1 further including, after processing said ~~silicon~~ substrate, fabricating ~~said~~ a final substrate surface using CMOS fabrication technique.

9. (original) A method of providing an array top oxide over an array of trenches containing trench capacitors and overlying vertical transistors comprising:

providing a substrate having an array area and a support area;

providing a sacrificial oxide layer over said array and support areas;

removing said sacrificial oxide layer only from said support area;

providing a gate oxide layer over said support area;

depositing a gate conductor layer over said array and support areas;

removing said gate conductor layer only from said array area;

depositing an array top oxide layer over said array and support areas; and

removing said array top oxide layer from said support area so as to leave remaining portions of said array top oxide layer only in said array area.

10. (Currently amended~~original~~) The method of claim 9 wherein said step of removing said sacrificial oxide layer only from said support area comprises:

removing said sacrificial oxide layer only from said support area wherein a first mask is provided over said array area to protect said array area during said sacrificial oxide layer removal processing; and

removing said first mask from said array area prior to providing said gate oxide layer over said support area.

11. (Currently amended~~original~~) The method of claim 10 wherein said step of removing said gate conductor layer only from said array area comprises:

removing said gate conductor layer only from said array area wherein a second mask is provided over said support area to protect said support area during said gate conductor layer removal processing; and

removing said second mask from said support area prior to depositing said array top oxide layer.

12. (original) The method of claim 11 wherein said first mask comprises a first etch support lithography mask and said second mask comprises a second etch support lithography mask.

13. (original) The method of claim 9 further including, prior to the step of removing sacrificial oxide layer, the steps of:

removing a pad nitride layer in both said array and support areas to expose a pad oxide layer in both said array and support areas;

removing at least a portion of said pad oxide layer from both said array and support areas; and

growing said sacrificial oxide layer over all exposed surface areas in both said array and support areas.

14. (original) The method of claim 9 wherein said step of removing said sacrificial oxide layer only from said support area prevents any out-diffusion from said array area.

15. (original) The method of claim 9 wherein said gate oxide layer is thermally grown over said support area, said array area being protected by said sacrificial oxide layer to prevent any out-diffusion from said array area.

16. (original) The method of claim 9 wherein said array top oxide layer is deposited by high-density plasma deposition.

17. (original) The method of claim 9 further including, removing said array top oxide layer from said support area by planarizing a surface of said substrate.

18. (Currently amended~~original~~) A method of providing an array top oxide over an array of trenches containing trench capacitors and overlying vertical transistors comprising:

providing a substrate including an array area and a support area,

said array area having an array of trenches containing trench capacitors overlying vertical transistors and having a surface over each of said trenches comprising a gate oxide of an adjacent isolation trench, electrically conductive contact, and nitride adjacent to said contact,

said support area having a plurality of regions of oxide isolation and a plurality of adjacent regions of nitride;

providing a sacrificial oxide layer over said array and support areas;

removing said nitride and a portion of said oxide from said array and support areas;

providing a first mask only over said array area;

removing said sacrificial oxide layer only from said support area, wherein said first mask protects said ~~underlying~~ array area to protect said trenches comprising said gate oxide, said electrically conductive contact, and said nitride adjacent to the contact in said array areas;

removing said first mask therein leaving remaining portions of said sacrificial oxide layer only over said array area;

providing a gate oxide layer only over said support area wherein said sacrificial oxide layer protects said array area so as to prevent alteration to said gate oxide in said array area;

depositing a gate conductor layer over said array and support areas;

providing a second mask only over said support area;

removing said gate conductor layer only from said array area, said second mask protecting said ~~underlying~~ support area during said gate conductor layer removal processing;

removing said second mask from said support area;

depositing an array top oxide layer over said array and support areas; and

removing said array top oxide layer from said support area to leave remaining portions of said array top oxide layer only in said array area.

19. (original) The method of claim 18 wherein said step of removing said sacrificial oxide layer only from said support area prevents arsenic out-diffusion from said array area.

20. (original) The method of claim 19 wherein said gate oxide layer is thermally grown over said support area, said array area being protected by said sacrificial oxide layer to further prevent any arsenic out-diffusion from said array area.